

# Design for Flip-Chip and Chip-Size Package Technology

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## Abstract

As new generations of electronic products emerge they often surpass the capability of existing packaging and interconnection technology and the infrastructure needed to support newer technologies. This movement is occurring at all levels: at the IC, at the IC package, at the module, at the hybrid, the PC board which ties all the systems together. Interconnection density and methodology becomes the measure of successfully managing performance. The gap between printed boards and semiconductor technology (wafer level integration) is greater than one order of magnitude in interconnection density capability, although the development of fine-pitch substrates and assembly technology has narrowed the gap somewhat. All viable efforts are being used in filling this void utilizing uncased integrated circuits (flip-chip) and incorporating more than one die or more than one part in the assembly process.

This paper provides a comparison of different commonly used technologies including flip-chip, chip-size and wafer level array package methodologies detailed in a new publication, IPC-7094. It considers the effect of bare die or die-size components in an uncased or minimally cased format, the impact on current component characteristics and reviews the appropriate PCB design guidelines to ensure efficient assembly processing. The focus of the IPC document is to provide useful and practical information to those who are considering the adoption of bare die or die size array components.

## Introduction

The flip-chip process was originally established for applications requiring aggressive miniaturization. Initially developed by IBM for the Solid Logic Technology (SLT) hybrid electronic circuitry for their System 360 computers, the die were very small and had very few contacts. The perimeter located bond sites were, as they are to a degree today, prepared with alloy bumps enabling the uncased semiconductor die to be bonded directly to a substrate using surface mount processes. In developing the IPC-7094, '*Design and Assembly Process Implementation for Flip-Chip and Die Size Components*', a number of experts were assembled to address the industries need for practical and up-to-date information and guidance in how to employ the uncased as well as minimally packaged semiconductor elements being offered to the commercial market. A number of miniature package solutions have evolved as well that retain an outline that is the same or very near the same as the die element. The uncased die element, when processed for in the wafer format for board level attachment, is identified as a wafer level BGA (WLBGA). A family of die-size BGA (DSBGA) is a component that employs a package assembly process utilizing an intermediate interposer to add a level of physical robustness, enable more efficient electrical test, burn-in and board level assembly.

Because of the rapid movement toward semiconductor package miniaturization, members of the Joint Electronic Device Engineering Council (JEDEC) developed a number of standards to help maintain a degree of uniformity for the semiconductor devices final configuration. Its membership includes semiconductor manufacturers, packaging services companies, material suppliers and users. The organizations JC-11 subcommittee is responsible for developing the mechanical outline requirements for solid state semiconductor packaging. The two standards that the IPC-7094 document has focused on are JEDEC 95 Publication 'Design Guide 4.18' (WLBGA) and 'Design Guide 4.7' for DSBGA. Their definition is as follows:

- A Wafer Level Ball Grid Array (WLBGA) has an array of metallic balls on the underside of the package. The substrate of the package is the semiconductor die with or without a redistribution layer that may have a square or rectangular shape with metallic balls applied onto the circuit side of the die. The array pattern of metallized balls provides the mechanical and electrical connection from the package body to the next level component such as a printed circuit board or intermediate substrate.
- A Die-size Ball Grid Array (DSBGA) also has an array of metallic balls on the underside of the package. The die elements are, however, attached to a dielectric substrate or carrier for redistribution of the die bond pads to a uniform contact array pattern. The package substrate may have a square or rectangular shape with a metallized circuit pattern applied to one or both sides of a dielectric structure. The size of the substrate or carrier is as close to the die size as practically possible.

The contacts on the WLBGA and DSBGA are balls, bumps or other protruding terminals constructed from a variety of alloy and/or polymer materials. The alloy ball or bump features are added to each contact site to provide the mechanical and electrical connection from the package body to the next level component such as a printed circuit board. Typically, when balls are present, they consist of eutectic lead/tin solder or a lead-free solder alloy. For purposes of the JEDEC documents, these contacts of whatever final form are referenced generically as “balls”. In regard to accommodation for board level assembly processing, the perimeter bumping process is generally limited to mounting uncased die having a relatively few contact sites. Larger die requiring higher pin count, will likely be processed to redistribute the peripheral located wire-bond sites to a uniform area array format. When the contact sites are arranged in the array package format it furnishes a more uniform interface configuration that better accommodates component level test, better access for circuit routing and is more compatibility with established surface mount assembly processes.

The profile height of the WLBGA and DSBGA devices are very thin. The finished devices are not encased in plastic typical of the coarser pitch BGA families, however, some suppliers may furnish these miniature components with a thin polymer coating to protect the exposed silicon surface. The actual height of the array device is defined as the distance from the seating plane (the surface of the mating circuit board) to the highest point on the package body. This distance is measured perpendicularly to the seating plane.

### Applications

Hand-held communication and entertainment products will continue to dominate the consumer markets worldwide and, with each generation offering more and more features and/or capability, system level integration and miniaturization becomes more of a priority. And even though the actual applications and functionality of the new product offering expands, the customer is expecting each generation to be smaller and lighter than its predecessor. Semiconductor elements widely targeted for improving package performance and package size reduction include both logic and memory. High volume consumer products requiring greater memory component density include:

- MP3 players, portable media players
- Memory cards (mini SD, SD, MMC etc.)
- Digital Still Cameras (DSC)
- Handheld video games
- Solid State Drives for mobile computing

Consumer applications may include a number of the functions unique to the product. For wireless handsets, for example, companies are looking for miniature package solutions for all functions.

Array packaging has evolved as the most direct method for package-to-board interface since there is no intermediate lead-frame required. The die prepared for flip-chip applications enables increased circuit density which can contribute to improved electrical performance. When comparing the WLBGA and DSBGA semiconductor packaging to the QFP lead-frame package, the surface area differences are quite dramatic. Table 1 provides a comparison of different semiconductor packaging methods having a common 10 mm x 10 mm die element with 100 active contact features.

**Table 1: Comparative Table of Various Technologies for a 100 I/O, 10x10 mm Size Die**

| Package parameter              | Bare Die (with wire bonds and pads) | Flip-chip               | QFP                 | DSBGA                 | FBGA                    |
|--------------------------------|-------------------------------------|-------------------------|---------------------|-----------------------|-------------------------|
| Contact pitch                  | 0.15 mm                             | 0.25 mm                 | 0.30 mm             | 0.50 mm               | 0.50 mm                 |
| Footprint area                 | 125 mm <sup>2</sup>                 | 120 mm <sup>2</sup>     | 750 mm <sup>2</sup> | 150 mm <sup>2</sup>   | 150 mm <sup>2</sup>     |
| Pkg/chip area                  | 1.0 mm <sup>2</sup>                 | 1.0 mm <sup>2</sup>     | 6.3 mm <sup>2</sup> | ≤ 1.1 mm <sup>2</sup> | ≥ 1.2 mm <sup>2</sup>   |
| Height                         | 0.4 to 0.6 mm                       | 0.5 to 0.7 mm           | 1.4 mm              | ≤ 1.0 mm              | ≥ 1.2 mm                |
| Inductance nH (circuit length) | 1 - 2 (0.75 mm wire)                | 0.1 – 0.2 (0.5 mm bump) | 1 – 7 (3 mm lead)   | 0.5 – 2.1 (1 mm ball) | 0.1 – 0.2 (1.2 mm ball) |
| Capacitance pF                 | 0.2                                 | 0.03                    | 0.5 – 1.0           | 0.05 – 0.2            | 0.05 – 0.3              |
| PCB attachment                 | epoxy + wire-bond                   | Solder + underfill      | Solder              | Solder                | Solder                  |

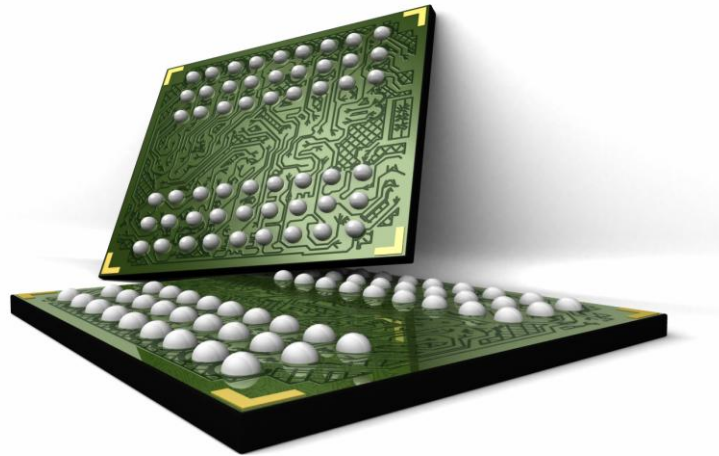
Source: IPC-7094

## WLBGA Challenges

Three primary factors that must be addressed when adopting WLBGA include; performance, reliability and cost. Although each factor carries equal status when assessing the merits of any flip-chip or re-distributed array packaging innovations, cost of the product will always influence adoption of one technology over the other. When companies choose to adopt uncased WLCSP semiconductors several issues should be considered:

- How to manage multiple IC vendors
- Availability of Known Good Die (test and burn-in)
- Die and wafer availability/uniform quality
- Compound yield expectation for less mature ICs
- Accommodating future die shrinks

A number of single-die wafer-level package innovations have been developed for a broad market; however, many supplier companies are not able to meet acceptable manufacturing yields. This is due in part to the difficulty of simultaneous testing of die while in the wafer format. The definition of KQD is that the supplier will demonstrate with data that the defect level and early failure rate estimates on die shipments are within the negotiated range, and retain a level of confidence in those estimates. Wafer level probe test is typically employed to perform only basic analysis and is not widely utilized for performance sorting, reliability screening or massively parallel contacting. If the uncased die elements are only to be tested while in the wafer format, the user still expects the same quality and reliability level of packaged part. The most thorough and reliable electrical testing is when bump or ball contacts are furnished on a singulated die element (see Figure 1), allowing each device to be socketed.



*Source: Micron Semiconductor*

**Figure 1. The uncased WLBGA, when prepared with compatible alloy bump contacts, can be socketed for electrical testing.**

The IPC-7094 document notes that, the term “Known Quality Die”, (KQD) does not depend on exact definitions of die quality and reliability in terms of defect levels or early failure rates, but instead offers the die supplier and user the opportunity to negotiate the price, quality and reliability targets needed to satisfy the system-level cost, yield and warranty requirements.

## Wafer Level Package Process Variations

The basic wafer level process begins with the under-bump (UB) metallization and bumping of the contact sites at the die perimeter. All of this work takes place while the die elements remain in the wafer-level format. The first metallization layer (typically chromium) is used to create a good bond to the aluminum pad initially prepared for the wire-bond processes. Subsequent metal films, typically copper and gold, are deposited to provide solderability for mounting the small ball contacts. It is common practice to first sputter an adhesion layer on in advance of the metals used to provide the required conductivity to the circuit. Adhesion-promoting metals include: nickel (Ni), molybdenum (Mo), chrome (Cr), tungsten (W), and titanium (Ti). These base materials are then over-plated with a more conductive metal such copper, gold, tin and palladium. Originally, the ball contact was an alloy of Au-Sn eutectic which melted at 360°C; therefore, the pad was called the ball-limiting metallurgy because the melted ball would not wet the glass passivation on the die surface beyond the area of the pad.

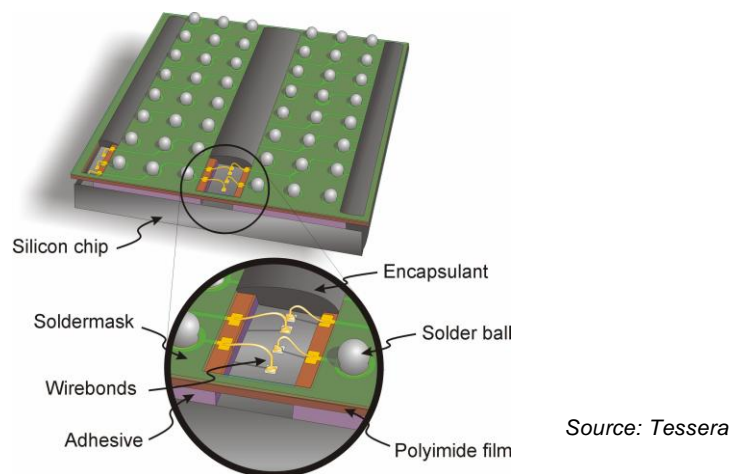
Later the Au-Sn ball contact was replaced by a Ni-Au plated solid copper ball attached with a Pb-Sn alloy to maintain a more uniform 'stand-off' height. The ball contact alloys of greatest favor today is SnPb eutectic or (for lead-free assembly) a SnAgCu composition.

Redistribution methods are utilized when the existing bond pad locations are not practical for board-level assembly. I/O redistribution is a sequential process where additional dielectric and conductive layers are added to the wafers active surface. The process can provide a uniform contact grid pattern that can enables a standard contact assignment to better facilitate component level testing and board or module level assembly. Dimensional control is a vital factor in the implementation of WLBGA assembly. Factors affecting the successful implementation of wafer-level processing are stabilized die element outline dimensions and wire-bond pad location and size. The metallization process allows the wire-bond sites to be routed to a uniform contact pitch to accommodate the ball or bump contact application. Process control in the bump or ball application process is paramount. Even small dimensional differences in bump profile and size can translate into uneven stress balance of the solder joining process that can affect end product reliability.

In regard to planning ahead for the potential of 'die shrink', suppliers often attempt to refine the die to gain higher yield or to enable additional units to be furnished within the fixed wafer area. With each revision or refinement, the die could shrink 5% to 10% in area, changing the die outline and often rearranging the wire-bond sites. This occurrence often leads to major redesign of the circuit board as well as the package substrate for the DSBGA. To minimize the impact of die shrink, all the active signal, power and ground contacts should be located in the die interior and locate any contacts used for redundant and/or mechanical support toward the outer area of the die. When the shrink occurs, the outer, less essential rows will be lost, but the critical contacts will not be affected. As the chip shrinks so does the 'Distance to the Neutral Point' (DNP), making the loss of redundant and mechanical contacts less of a reliability issue. With this approach, the next level of assembly is not affected as the non-critical connections simply become open pins. If the die undergoes excessive shrinks the contact array matrix will likely need to be re-established with a reduced contact pitch and contact size.

### Die Size Array Package Assembly Process

Die size (DSBGA) array package technology has evolved using widely differing constructions including a number of proprietary packaging methodologies. Many applications have been successful in employing flip-chip technology, however, when handling and testing the uncased die, users realize that without some form of reinforcement (post assembly underfill or encapsulation) that they are prone to cracking and, because of the thermal co-efficient of expansion differences of silicon and PCB laminates, solder joint fatigue is common. Companies have found that even minimal packaging of the bare die element can reduce assembly process damage. Although DSBGA package methods differ somewhat, a number of companies offer a structure that enhances both functional performance and physical robustness. One of the most widely adopted packaging processes used for packaging silicon is the face-down wire-bond  $\mu$ BGA<sup>®</sup>. The technology enables the smallest possible finished package outline while providing a method for furnishing a uniform contact size. Although the use of the methodology requires a licensing agreement with the patent holder, the material set used in the package process significantly contributes to the physical integrity of the end product (illustrated in Figure 2).



**Figure 2. Face-down DSBGA with through-slot wire bond interconnect**

The  $\mu$ BGA package methodology was developed to minimize the impact of the thermal coefficient of expansion between the silicon die element and the circuit board.

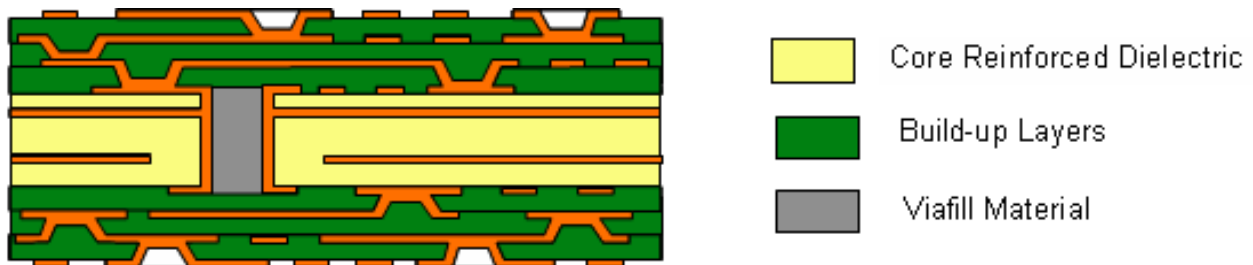
When completed, the structure provides a unique compliant polymer adhesive layer between the die surface and package substrate to decouple the differential expansion of the silicon (3ppm per °C) from that of the circuit board substrate (~16ppm per °C). The package, when mounted to the circuit board, does not require underfill.

### High Density Circuit Routing

Board design for WLBGA and DSBGA is similar to that presently used for soldered surface mount assembly, however, land pattern sizes will shrink and circuit density will likely increase. To provide the performance and interconnection capability needed for flip-chip and chip-scale IC packaging it will require adapting higher density circuit board fabrication technology. For the uncased die, for example, the contact sites are typically designed for wire-bond processing and are often randomly spaced at the die periphery and will also be a great deal smaller than those used for array packaged ICs (the die element with 100 micron pitch peripheral configured bond sites will likely have a pad size of 50 x 50 microns). Arrays configured devices, on the other hand, are generally more uniform and can be configured with a much larger contact geometry and wider spacing between contact features. When establishing the array format the package designers will first consider a contact pitch that can be efficiently routed on the circuit board. In addition to the basic electrical connections, several bump contacts may be added for heat dissipation, mechanical support (outriggers, chip orientation, or future design migration). To enhance performance, the package designer may determine that the product will need redundant bump contacts for power, ground and critical signals. The actual number of bump or ball contacts needed varies with electrical, thermal, and mechanical requirements.

After establishing the land pattern array it's up to the PCB design specialist to plan optimum component placement and alternative circuit routing strategies. Two fabrication methodologies can be considered; the more traditional drilled and plated via hole fabrication process or the use of micro-via-in-land build-up board technology. Signal routing on subsurface layers of the drilled via PCB will be restricted by the space reserved between via pad sites. Adding more circuit layers can enable higher component density but, the added layers may increase the thickness of the substrate and extend fabrication complexity. On the other hand, finer circuit lines and spaces, although reducing the need for added circuit layers, may prove to be more costly due to the lower fabrication yield. As the pin count increases on smaller array packages, it may be necessary to move away from the conventional drilled-hole multilayer PCB fabrication technology to more advanced fabrication technologies. To maximize the efficiency of the circuit structure surface, the designer may consider build-up fabrication, moving the via-hole onto the land pattern for more efficient subsurface circuit routing. The blind plated micro-via within the land pattern can provide circuit routing density that is far greater than that possible with conventional drilled-through-hole fabrication alone.

The micro-via plated hole typically interconnects only component land patterns on the outer surface circuit layer to one or more subsurface circuit layers. The build-up of high density circuit layers with laser drilled and plated micro-vias for layer-to-layer interconnect (typical of that illustrated in Figure 3) enables the developer to maximize circuit density and performance while reducing circuit layers and minimizing overall product or module size.



Source: IPC-7094

**Figure 3. Ten layer (3+4+3) build-up substrate example.**

The micro-via hole-in-land can be, and most often is, much smaller than the conventional mechanically drilled and plated through-hole via. Moving the via hole onto the land pattern enables much closer component spacing and the smaller size hole allows significantly greater circuit routing channels on the inner layers of the circuit structure.

### Land Pattern Planning

After establishing the contact type (ball or bump) and diameter, the supplier will determine the appropriate contact feature geometry and pitch.

Although the land patterns developed for spherical (ball) contacts can be the same diameter as the sphere, experts recommend a land diameter that is slightly smaller, however, with lower profile ‘bump’ contacts, the land pattern diameter is more likely to be the same as the bump diameter. Because there is little time for the user to build, test and evaluate land pattern variations for each device, JEDEC has stated that the IC supplier is obligated to specify the recommended land pattern geometry that will furnish the most satisfactory electrical interface between the device and package interposer or module substrate. The printed board land pattern for flip-chips and die size array packages is simply a circle of coated copper foil whose diameter is the same or slightly smaller than the bump or ball contact diameter. Table 2 compares variations of contact features recommended in IPC-7094.

**Table 2: Contact pitch, ball size to land pattern approximation (microns)**

| Contact pitch | Nominal bump or ball diameter | Land diameter reduction | Nominal land size | Land size variation |
|---------------|-------------------------------|-------------------------|-------------------|---------------------|
| 500           | 300                           | 20%                     | 250               | 200 – 250           |
| 400           | 250                           | 20%                     | 200               | 170 - 200           |
| 300           | 200                           | 20%                     | 150               | 120 - 150           |
| 250           | 150                           | 10%                     | 125               | 100 - 125           |

Source: IPC-7094

The requirements for design and the fabrication options used to develop circuit board substrates are well defined in IPC-2221. In addition, when the core material reflects requirements identified in the sectional standards; IPC-2222, IPC-2223, IPC-2224, IPC-2225 and IPC-2226 (the IPC-2226 is specifically targeted for high-density interconnect applications). The standard series provide recommendations for signal, power, ground and mixed distribution layers, dielectric separation, via formation and metallization requirements and other design features that are necessary for HDI and advanced IC interconnection substrates including trade-off analyses required to match the mounting structure to the selected chip set. While lithography technologies establish the general limitations for circuit feature sizes, each of the various types of substrate has slightly different limits based on their construction and each has its own strengths and weaknesses in terms of layering and drilling. Table 3 lists three key characteristics of today’s electronic package and module substrates and identifies the current status for high volume manufacturing capability around the globe.

**Table 3: Substrate Design Feature Characteristics**

| DESIGN FEATURES   | CONVENTIONAL | LEADING EDGE | STATE-OF-THE-ART       |
|---|--------------|--------------|------------------------|
| Lines & Spaces (µm)   | 100 - 250    | 50 – 100     | < 25                   |
| Via Diameter (µm; as drilled)                                 | >250         | 100 - 200    | 50                     |
| (Conductive) Layer Count                                      | 2 - 6        | 8 - 20       | >20                    |
| Dielectric Thickness (µm)                                     | 25 - 100     | 12 -25       | 12                     |
| Conductor Thickness (µm)                                      | 18 -36       | 10 -17       | 8 - 9                  |
| Adhesive  | Yes          | Adhesiveless | Adhesiveless           |
| Minimum Annular Ring =(pad diameter-hole diameter) x 1/2 (µm) | 200          | 50           | None<br>(landless via) |

Source: IPC Industry Roadmap

**Design for Assembly Processing**

As noted, PCB design for WLBGA and DSBGA assembly is similar to that for presently used for soldered surface mount assembly except, in some specialized applications the WLBGA die may adapt a non-solder process for attachment.

Key issues that need to be established for device mounting during the design planning phase of the substrate or module development are:

- Land pattern geometry
- Solder mask material, clearances
- Surface plating compatibility for attachment
- Clearance required for mounting, inspection
- Assembly test method, test feature requirement
- Thermal management, heat dissipation

To accommodate precise registration of the stencil for solder paste printing and ensure accurate component placement, some means of vision or camera assisted alignment is required. Features needed for accurate positional reference on the PCB surface are fiducial targets. Both global and local fiducial targets are needed to enable assembly process efficiency. The globally located fiducial targets are used for both precise stencil-to-board alignment ensuring accurate solder paste print registration and, in subsequent process steps, to assist in the placement of both passive and active surface mount devices. When smaller boards are furnished in a panel format, three fiducial targets are recommended near the edge of the panel. The example furnished in the IPC-7094 document recommends the establishment one fiducial in the corner area of the PCB unit as a 0-0 reference with two additional fiducial targets extended outward at a 90 angle in the X and Y directions. These targets are used to enable more precise automated device placement by correcting offsets (X and Y position) and rotational offsets (theta position). In addition, one or preferably two targets are to be provided within the mounting zone for fine-pitch devices. Additional 'zonal' fiducial target features may be required on larger boards having exceptionally high quantities of passive and active devices. A common fiducial size is preferred at all locations, although shape and size can be customized for unique applications. The Surface Mount Equipment Manufacturers Association (SMEMA) members, however, have agreed and recommend the use of a 1.0mm (.040") diameter solid land. The fiducial surface may be plated or non-plated and they must be relatively flat and free of solder mask to ensure that the camera can make a quick identification.

Additionally, palletizing smaller and/or odd shaped circuit boards is a common technique used to improve assembly efficiency. To accommodate de-paneling and electrical testing, each board unit within the panel should be furnished with a minimum of two tooling holes (preferably in diagonal corners). The hole size is typically defined by the assembly specialist (0.65 mm diameter is common) and they should be specified to be free of plating to ensure a more precise finished hole diameter.

### **Conclusion**

Feature sizes for WLPGA and DSBGA packages will continue to shrink as the silicon fabrication technology adopts significantly higher circuit densities. This trend will allow the IC designer to further compress the functionality onto even smaller die outlines. To maintain the minimal finished package outline it will be necessary to reduce the contact size and move the contact features closer together. We can expect the next generation of these components to push the limits of printed circuit fabrication capability. In preparation for higher density circuit boards, designers and suppliers will need to work together in selecting the best laminate materials and adopt more advanced fabrication processes. Even today, the higher density circuit routing and contact features are very near the size of early semiconductor technology, prompting circuit fabrication specialist to employ more sophisticated clean-room enclosures around key processes. For example, any microscopic particles at any stage of the circuit fabrication environment will have the potential to cause fatal defects. The photo-lithographic process steps in particular and the preparation steps leading up to the process are particularly vulnerable to particle contamination. Additionally, surface contamination or incompatible surface finish on the substrate is a concern because they can potentially contribute to product failure. In regard to market acceptance and performance of WLPGA and DSBGA technology, there remain significant challenges that need to be addressed:

- Aggressive cost reduction strategies
- Consistency of die level quality
- Refining wafer and component level test capability
- PCB design analysis and assembly modeling capabilities
- Reliability improvement strategies

In regard to package and module assembly, there will be an ongoing need for the OEM or EMS provider to make capital improvements to their facility. Improvements in the form of a cleaner environment for each process and significantly greater accuracy in solder printing, device placement and solder process control.

**References:**

1. IPC-7094, '*Design and Assembly Process Implementation for Flip-Chip and Die Size Components*'
2. IPC-2220, '*Design Standard Series including IPC-2221, IPC-2222, IPC-2223 and IPC-2225*'
3. IPC-2226, '*Design Standard for High Density Interconnect (HDI) Printed Boards*'
4. JEDEC Publication 95 Section 4.7, '*Die-Size Ball Grid Array Package (DSBGA)*'
5. JEDEC Publication 95 Section 4.18, '*Wafer Level Ball Grid Arrays (WLBGA)*'

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